查询ASM5I9773A供应商

2.5V or 3.3V, 200-MHz, 12-Output Zero Delay Buffer

Features

- Output frequency range: 8.33MHz to 200MHz
- Input frequency range: 6.25MHz to 125MHz
- 2.5V or 3.3V operation
- Split 2.5V / 3.3V outputs
- ±2%(max) Output duty cycle variation
- 12 Clock outputs: drive up to 24 clock lines
- One feedback output
- Three reference clock inputs: LVPECL or LVCMOS
- 300pS (max) output-output skew
- Phase-locked loop (PLL) bypass mode
- 'SpreadTrak'
- Output enable/disable
- Pin-compatible with CY29773, MPC9773 and MPC973
- Industrial temperature range: –40°C to +85°C
- 52pin 1.0mm TQFP package
- RoHS Compliance

Functional Description

The ASM5I9773A is a low-voltage high-performance 200-MHz PLL-based zero delay buffer designed for high speed clock distribution applications.

The ASM5I9773A features one LVPECL and two LVCMOS reference clock inputs and provides 12 outputs partitioned in three banks of four outputs each. Each bank divides the VCO output per SEL(A:C) settings (see Table 2. Function Table (Configuration Controls)). These dividers allow output-to-input ratios of 8:1, 6:1, 5:1, 4:1, 3:1, 8:3, 5:2, 2:1, 5:3, 3:2, 4:3, 5:4, 1:1, and 5:6. Each LVCMOS-compatible output can drive 50Ω series- or parallel-terminated transmission lines. For series-terminated transmission lines, each output can drive one or two traces, giving the device an effective fanout of 1:24.

The PLL is ensured stable, given that the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies, from 8 MHz to 200 MHz. For normal operation, the external feedback input FB_IN is connected to the feedback output FB_OUT. The internal VCO is running at multiples of the input reference clock set by the feedback divider (see Table 1. Frequency Table).

When PLL_EN is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

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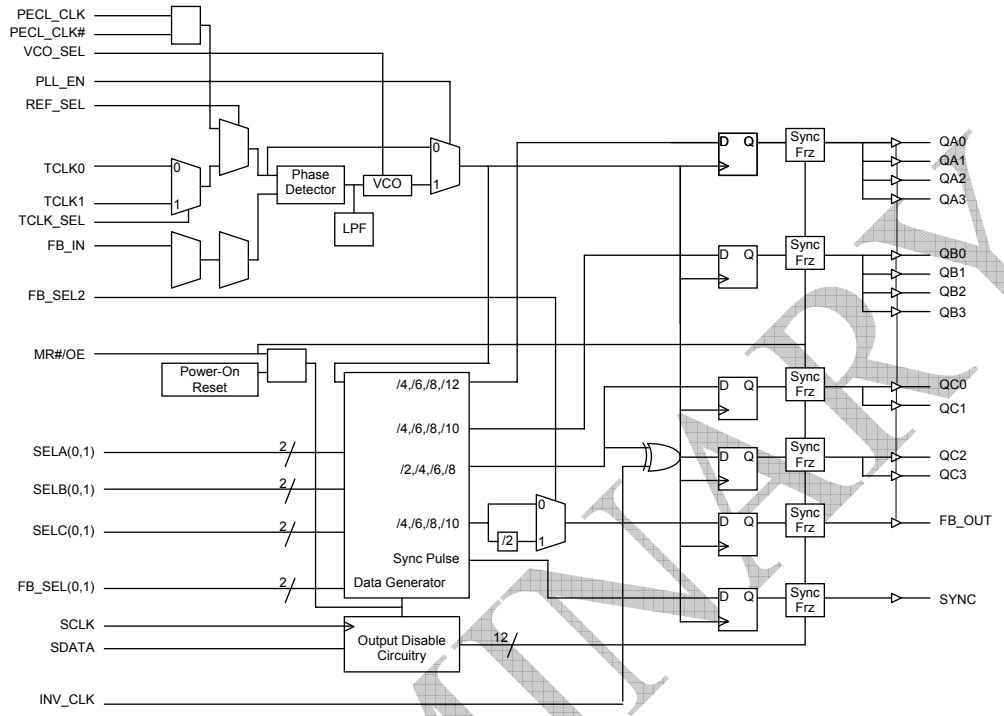
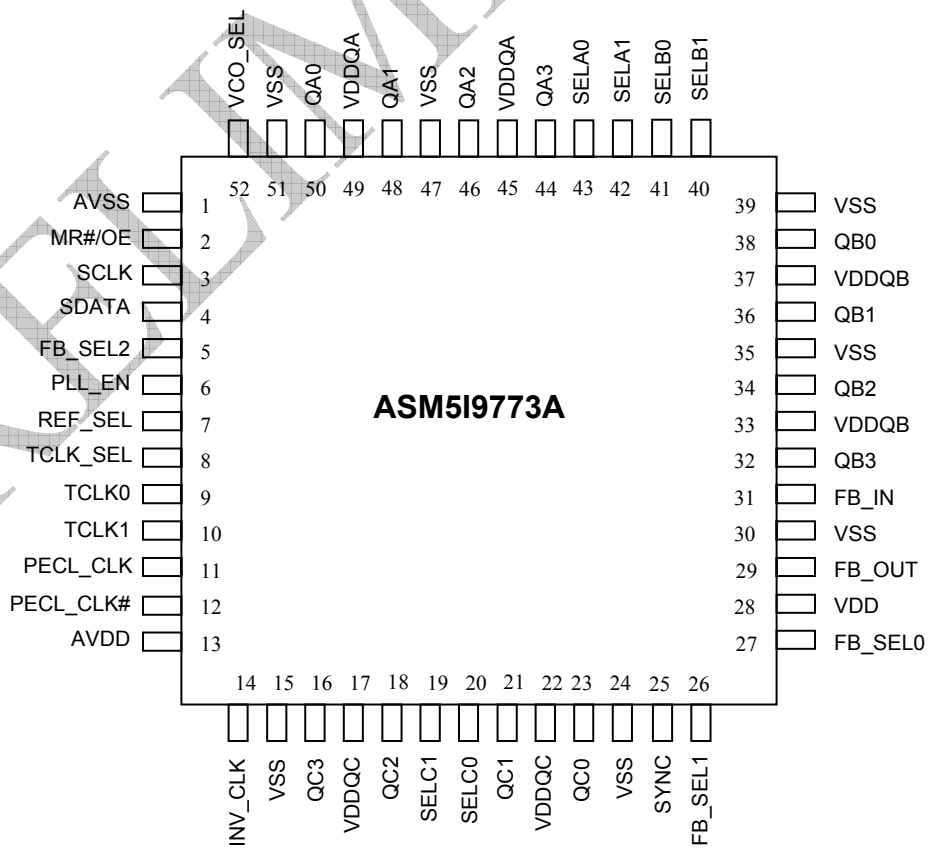
Block Diagram



Pin Configuration



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Pin Configuration[1]

Pin	Name	I/O	Type	Description
11	PECL_CLK	I, PU	LVPECL	**LVPECL reference clock input**.
12	PECL_CLK#	I	LVPECL	**LVPECL reference clock input**.
9	TCLK0	I, PU	LVCMOS	**LVCMOS/LVTTL reference clock input**.
10	TCLK1	I, PU	LVCMOS	**LVCMOS/LVTTL reference clock input**.
44,46,48,50	QA(3:0)	O	LVCMOS	**Clock output bank A**.
32,34,36,38	QB(3:0)	O	LVCMOS	**Clock output bank B**.
16,18,21,23	QC(3:0)	O	LVCMOS	**Clock output bank C**.
29	FB_OUT	O	LVCMOS	**Feedback clock output**. Connect to FB_IN for normal operation.
31	FB_IN	I, PU	LVCMOS	**Feedback clock input**. Connect to FB_OUT for normal operation. This input should be at the same voltage rail as input reference clock. See *Table 1. Frequency Table*.
25	SYNC	O	LVCMOS	**Synchronous pulse output**. This output is used for system synchronization.
6	PLL_EN	I, PU	LVCMOS	**PLL enable/bypass input**. When Low, PLL is disabled/bypassed and the input clock connects to the output dividers.
2	MR#/OE	I, PU	LVCMOS	**Master reset and Output enable/disable input**. See *Table 2. Function Table (Configuration Controls)*.
8	TCLK_SEL	I, PU	LVCMOS	**LVCMOS Clock reference select input**. See *Table 2. Function Table (Configuration Controls)*.
7	REF_SEL	I, PU	LVCMOS	**LVCMOS/LVPECL Reference select input**. See *Table 2. Function Table (Configuration Controls)*.
52	VCO_SEL	I, PU	LVCMOS	**VCO Operating frequency select input**. See *Table 2. Function Table (Configuration Controls)*.
14	INV_CLK	I, PU	LVCMOS	**QC(2,3) Phase selection input**. See *Table 2. Function Table (Configuration Controls)*.
5,26,27	FB_SEL(2:0)	I, PU	LVCMOS	**Feedback divider select input**. See *Table 6*.
42,43	SELA(1,0)	I, PU	LVCMOS	**Frequency select input, Bank A**. See *Table 3. Function Table (Bank A)*.
40,41	SELB(1,0)	I, PU	LVCMOS	**Frequency select input, Bank B**. See *Table 4. Function Table (Bank B)*.
19,20	SELC(1,0)	I, PU	LVCMOS	**Frequency select input, Bank C**. See *Table 5. Function Table (Bank C)*.
3	SCLK	I, PU	LVCMOS	**Serial clock input**.
4	SDATA	I, PU	LVCMOS	**Serial data input**.
45,49	VDDQA	Supply	VDD	**2.5V or 3.3V Power supply for bank A output clocks**[2,3].
33,37	VDDQB	Supply	VDD	**2.5V or 3.3V Power supply for bank B output clocks**[2,3].
22,17	VDDQC	Supply	VDD	**2.5V or 3.3V Power supply for bank C output clocks**[2,3].
13	AVDD	Supply	VDD	**2.5V or 3.3V Power supply for PLL**[2,3].
28	VDD	Supply	VDD	**2.5V or 3.3V Power supply for core and inputs**[2,3].
1	AVSS	Supply	Ground	**Analog Ground**.
15,24,30,35, 39,47,51	VSS	Supply	Ground	**Common Ground**.

Notes:
1. PU = Internal pull up, PD = Internal pull down.
2. A 0.1µF bypass capacitor should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the traces.
3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQA, VDDQB, and VDDQC power supply pins.

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'SpreadTrak'

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. ASM5I9773A is designed so as not to filter off the Spread Spectrum feature of the Reference Input, assuming it exists.

When a zero delay buffer is not designed to pass the Spread Spectrum feature through, the result is a significant amount of tracking skew which may cause problems in the systems requiring synchronization.

Table 1: Frequency Table

Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3V)	Input Frequency Range (AVDD = 2.5V)
÷4	Input Clock * 4	50 MHz to 125 MHz	50 MHz to 95 MHz
÷6	Input Clock * 6	33.3 MHz to 83.3 MHz	33.3 MHz to 63.3 MHz
÷8.	Input Clock * 8	25 MHz to 62.5 MHz	25 MHz to 47.5 MHz
÷10	Input Clock * 10	20 MHz to 50 MHz	20 MHz to 38 MHz
÷12	Input Clock * 12	16.6 MHz to 41.6 MHz	16.6 MHz to 31.6 MHz
÷16	Input Clock * 16	12.5 MHz to 31.25 MHz	12.5 MHz to 23.75 MHz
÷20	Input Clock * 20	10 MHz to 25 MHz	10 MHz to19 MHz
÷24	Input Clock * 24	8.3 MHz to 20.8 MHz	8.3 MHz to 15.8 MHz
÷32	Input Clock * 32	6.25 MHz to 15.625 MHz	6.25 MHz to 11.8 MHz
÷40	Input Clock * 40	5 MHz to 12.5 MHz	5 MHz to 9.5 MHz

Table 2. Function Table (Configuration Controls)

Control	Default	0	1
REF_SEL	1	TCLK0, TCLK1	PECL_CLK
TCLK_SEL	1	TCLK0	TCLK1
VCO_SEL	1	VCO÷2 (low input frequency range)	VCO÷1 (high input frequency range)
PLL_EN	1	Bypass mode, PLL disabled. The input clock connects to the output dividers	PLL enabled. The VCO output connects to the output dividers
INV_CLK	1	QC2 and QC3 are in phase with QC0 and QC1	QC2 and QC3 are inverted (180° phase shift) with respect to QC0 and QC1
MR#/OE	1	Outputs disabled (three-state) and reset of the device. During reset/output disable the PLL feedback loop is open and the VCO running at its minimum frequency. The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled

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Table 3. Function Table (Bank A)

VCO_SEL	SELA1	SELA0	QA(0:3)
0	0	0	÷8
0	0	1	÷12
0	1	0	÷16
0	1	1	÷24
1	0	0	÷4
1	0	1	÷6
1	1	0	÷8
1	1	1	÷12

Table 4. Function Table (Bank B)

VCO_SEL	SELB1	SELB0	QB(0:3)
0	0	0	÷8
0	0	1	÷12
0	1	0	÷16
0	1	1	÷20
1	0	0	÷4
1	0	1	÷6
1	1	0	÷8
1	1	1	÷10

Table 5. Function Table (Bank C)

VCO_SEL	SELC1	SELC0	QC(0:3)
0	0	0	÷4
0	0	1	÷8
0	1	0	÷12
0	1	1	÷16
1	0	0	÷2
1	0	1	÷4
1	1	0	÷6
1	1	1	÷8

Table 6. Function Table (FB_OUT)

VCO_SEL	FB_SEL2	FB_SEL1	FB_SEL0	FB_OUT
0	0	0	0	÷8
0	0	0	1	÷12
0	0	1	0	÷16
0	0	1	1	÷20
0	1	0	0	÷16
0	1	0	1	÷24
0	1	1	0	÷32
0	1	1	1	÷40
1	0	0	0	÷4
1	0	0	1	÷6
1	0	1	0	÷8
1	0	1	1	÷10
1	1	0	0	÷8
1	1	0	1	÷12
1	1	1	0	÷16
1	1	1	1	÷20

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
VDD	DC Supply Voltage		–0.3	5.5	V
VDD	DC Operating Voltage	Functional	2.375	3.465	V
V_{IN}	DC Input Voltage	Relative to VSS	–0.3	VDD+ 0.3	V
V_{OUT}	DC Output Voltage	Relative to VSS	–0.3	VDD+ 0.3	V
V_{TT}	Output termination Voltage			VDD ÷2	V
LU	Latch-up Immunity	Functional	200	-	mA
R_{PS}	Power Supply Ripple	Ripple Frequency < 100 kHz		150	mVp-p
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
T_J	Temperature, Junction	Functional		+150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Functional		23	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	Functional		55	°C/W
ESD_H	ESD Protection (Human Body Model)		2000		V
FIT	Failure in Time	Manufacturing test	10		ppm

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

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DC Electrical Specifications (VDD = 2.5V ± 5%, T_A = – 40°C to + 85°C)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input Voltage, Low	LVCMOS	-	-	0.7	V
V_{IH}	Input Voltage, High	LVCMOS	1.7	-	VDD+0.3	V
V_{PP}	Peak-Peak Input Voltage	LVPECL	250	-	1000	mV
V_{CMR}	Common Mode Range [4]	LVPECL	1.0	-	VDD – 0.6	V
V_{OL}	Output Voltage, Low [5]	I_{OL}= 15 mA	-	-	0.6	V
V_{OH}	Output Voltage, High [5]	I_{OH}= –15 mA	1.8	-	-	V
I_{IL}	Input Current, Low [5]	V_{IL}= VSS	-	-	-100	µA
I_{IH}	Input Current, High[6]	V_{IL}= VDD	-	-	100	µA
I_{DDA}	PLL Supply Current	AVDD only	-	5	10	mA
I_{DDQ}	Quiescent Supply Current	All VDD pins except AVDD	-	-	8	mA
I_{DD}	Dynamic Supply Current	Outputs loaded @ 100 MHz	-	135	-	mA
C_{IN}	Input Pin Capacitance		-	4	-	pF
Z_{OUT}	Output Impedance		14	18	22	Ω

DC Electrical Specifications (VDD = 3.3V ± 5%, T_A = – 40°C to + 85°C)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input Voltage, Low	LVCMOS	-	-	0.8	V
V_{IH}	Input Voltage, High	LVCMOS	2.0	-	VDD+0.3	V
V_{PP}	Peak-Peak Input Voltage	LVPECL	250	-	1000	mV
V_{CMR}	Common Mode Range[4]	LVPECL	1.0	-	VDD– 0.6	V
V_{OL}	Output Voltage, Low[5]	I_{OL}= 24 mA	-	-	0.55	V
		I_{OL}= 12 mA	-	-	0.30	
V_{OH}	Output Voltage, High[5]	I_{OH}= –24 mA	2.4	-	-	V
I_{IL}	Input Current, Low [6]	V_{IL}= VSS	-	-	-100	µA
I_{IH}	Input Current, High[6]	V_{IL}= VDD	-	-	100	µA
I_{DDA}	PLL Supply Current	AVDD only	-	5	10	mA
I_{DDQ}	Quiescent Supply Current	All VDD pins except AVDD	-	-	8	mA
I_{DD}	Dynamic Supply Current	Outputs loaded @ 100 MHz	-	225	-	mA
C_{IN}	Input Pin Capacitance		-	4	-	pF
Z_{OUT}	Output Impedance		12	15	18	Ω

Notes:
4. V_{CMR} (DC) is the crossing point of the differential input signal. Normal operation is obtained when the crossing point is within the V_{CMR} range and the input swing is within the V_{PP} (DC) specification.
5. Driving one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50 Ω series terminated transmission lines.
6. Inputs have pull-up or pull-down resistors that affect the input current.

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AC Electrical Specifications (VDD = 2.5V ±5%, T_A = –40°C to +85°C)[7]

Parameter	Description	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO Frequency		200	-	380	MHz
f_{in}	Input Frequency	÷4 Feedback	50	-	95	MHz
		÷6 Feedback	33.3	-	63.3	
		÷8 Feedback	25	-	47.5	
		÷10 Feedback	20	-	38	
		÷12 Feedback	16.6	-	31.6	
		÷16 Feedback	12.5	-	23.75	
		÷20 Feedback	10	-	19	
		÷24 Feedback	8.3	-	15.8	
		÷32 Feedback	6.25	-	11.8	
		÷40 Feedback	5	-	9.5	
		Bypass mode (PLL_EN = 0)	0	-	200	
f_{refDC}	Input Duty Cycle		25	-	75	%
V_{PP}	Peak-Peak Input Voltage	LVPECL	500	-	1000	mV
V_{CMR}	Common Mode Range[8]	LVPECL	1.2	-	VDD– 0.6	V
t_r, t_f	TCLK Input Rise/FallTime	0.7V to 1.7V	-	-	1.0	nS
f_{MAX}	Maximum Output Frequency	÷2 Output	100	-	190	MHz
		÷4 Output	50	-	95	
		÷6 Output	33.3	-	63.3	
		÷8 Output	25	-	47.5	
		÷10 Output	20	-	38	
		÷12 Output	16.6	-	31.6	
		÷16 Output	12.5	-	23.75	
		÷20 Output	10	-	19	
		÷24 Output	8.3	-	15.8	
f_{SCLK}	Serial Clock Frequency		-	-	20	MHz
DC	Output Duty Cycle	f_{MAX} < 100 MHz	47.5	-	52.5	%
		f_{MAX} > 100 MHz	45	-	55	
t_r, t_f	Output Rise/Fall times	0.6V to 1.8V	0.1	-	1.0	nS
$t_{(\varphi)}$	Propagation Delay (static phase offset)	TCLK to FB_IN	-125	-	125	pS
		PCLK to FB_IN	-125	-	125	

Notes:
7. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Outputs are at same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.
8. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of VCMR or VPP impacts static phase offset $t_{(\varphi)}$.

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AC Electrical Specifications (VDD = 2.5V ± 5%, T_A = – 40°C to + 85°C)[9]

Parameter	Description	Condition	Min	Typ	Max	Unit
$t_{sk(O)}$	Output-to-Output Skew	Skew within Bank A	-	-	75	pS
		Skew within Bank B	-	-	100	
		Skew within Bank C	-	-	150	
$t_{sk(B)}$	Bank-to-Bank Skew		-	-	400	pS
$t_{PLZ, HZ}$	Output Disable Time		-	-	10	nS
$t_{PZL, ZH}$	Output Enable Time		-	-	10	nS
BW	PLL Closed Loop Bandwidth (-3dB)	÷4 Feedback	-	1.3 - 2.0	-	MHz
		÷6 Feedback	-	0.7 - 1.3	-	
		÷8 Feedback	-	0.9 - 1.3	-	
		÷10 Feedback	-	0.6 - 1.1	-	
		÷12 Feedback	-	0.6 - 0.9	-	
		÷16 Feedback	-	0.4 - 0.6	-	
		÷20 Feedback	-	0.6 - 0.9	-	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency (125 MHz) RMS (1σ)	-	7	30	pS
		Same frequency	-	-	150	
		Multiple frequencies	-	-	435	
$t_{JIT(PER)}$	Period Jitter	Same frequency (125 MHz) RMS (1σ)	-	6	30	pS
		Same frequency	-	45	75	
		Multiple frequencies	-	-	235	
$t_{JIT(\varphi)}$	I/O Phase Jitter		-	-	150	pS
t_{LOCK}	Maximum PLL Lock Time		-	-	1	mS

Notes:

9. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Outputs are at same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.

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AC Electrical Specifications (VDD = 3.3V ± 5%, TA = – 40°C to + 85°C)[10]

Parameter	Description	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO Frequency		200	-	500	MHz
f_{in}	Input Frequency	÷4 Feedback	50	-	125	MHz
		÷6 Feedback	33.3	-	83.3	
		÷8 Feedback	25	-	62.5	
		÷10 Feedback	20	-	50	
		÷12 Feedback	16.6	-	41.6	
		÷16 Feedback	12.5	-	31.25	
		÷20 Feedback	10	-	25	
		÷24 Feedback	8.3	-	20.8	
		÷32 Feedback	6.25	-	15.625	
		÷40 Feedback	5	-	12.5	
		Bypass mode (PLL_EN = 0)	0	-	200	
f_{refDC}	Input Duty Cycle		25	-	75	%
V_{PP}	Peak-Peak Input Voltage	LVPECL	500	-	1000	mV
V_{CMR}	Common Mode Range[8]	LVPECL	1.2	-	VDD–0.9	V
t_r, t_f	TCLK Input Rise/FallTime	0.8V to 2.0V	-	-	1.0	nS

Notes:

10. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Outputs are at same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.

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AC Electrical Specifications (VDD = 3.3V ±5%, T_A = –40°C to +85°C)[11]

Parameter	Description	Condition	Min	Typ	Max	Unit
f_{MAX}	Maximum Output Frequency	÷2 Output	100	-	200	MHz
		÷4 Output	50	-	125	
		÷6 Output	33.3	-	83.3	
		÷8 Output	25	-	62.5	
		÷10 Output	20	-	50	MHz
		÷12 Output	16.6	-	41.6	
		÷16 Output	12.5	-	31.25	
		÷20 Output	10	-	25	
		÷24 Output	8.3	-	20.8	
f_{SCLK}	Serial Clock Frequency		-	-	20	MHz
DC	Output Duty Cycle	f_{MAX} < 100 MHz	48	-	52	%
		f_{MAX} > 100 MHz	45	-	55	
t_r, t_f	Output Rise/Fall times	0.55V to 2.4V	0.1	-	1.0	nS
t(φ)	Propagation Delay (static phase offset)	TCLK to FB_IN, same VDD	-125	-	125	pS
		PCLK to FB_IN, same VDD	-125	-	125	
$t_{sk(O)}$	Output-to-Output Skew	Skew within Bank A	-	-	75	pS
		Skew within Bank B	-	-	100	
		Skew within Bank C	-	-	150	
$t_{sk(B)}$	Bank-to-Bank Skew		-	-	325	pS
$t_{PLZ, HZ}$	Output Disable Time		-	-	8	nS
$t_{PZL, ZH}$	Output Enable Time		-	-	8	nS
BW	PLL Closed Loop Bandwidth (–3 dB)	÷4 Feedback	-	1.3–2.0	-	MHz
		÷6 Feedback	-	0.7–1.3	-	
		÷8 Feedback	-	0.9–1.3	-	
		÷10 Feedback	-	0.6–1.1	-	
		÷12 Feedback	-	0.6–0.9	-	
		÷16 Feedback	-	0.4–0.6	-	
		÷20 Feedback	-	0.6–0.9	-	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency (125 MHz) RMS (1σ)	-	7	30	pS
		Same frequency	-	-	100	
		Multiple frequencies	-	-	375	
$t_{JIT(PER)}$	Period Jitter	Same frequency (125 MHz) RMS (1σ)	-	6	30	pS
		Same frequency	-	45	75	
		Multiple frequencies	-	-	225	
$t_{JIT(φ)}$	I/O Phase Jitter	I/O same VDD	-	-	150	pS
t_{LOCK}	Maximum PLL Lock Time		-	-	1	mS

Notes:
11. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Outputs are at same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.

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SYNC Output

In situations where output frequency relationships are not integer multiples of each other the SYNC output provides a signal for system synchronization. The ASM5I9773A monitors the relationship between the QA and the QC output clocks. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse depend on the higher of the QA and QC output frequencies. The following timing diagram illustrates various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the QA and QC outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.

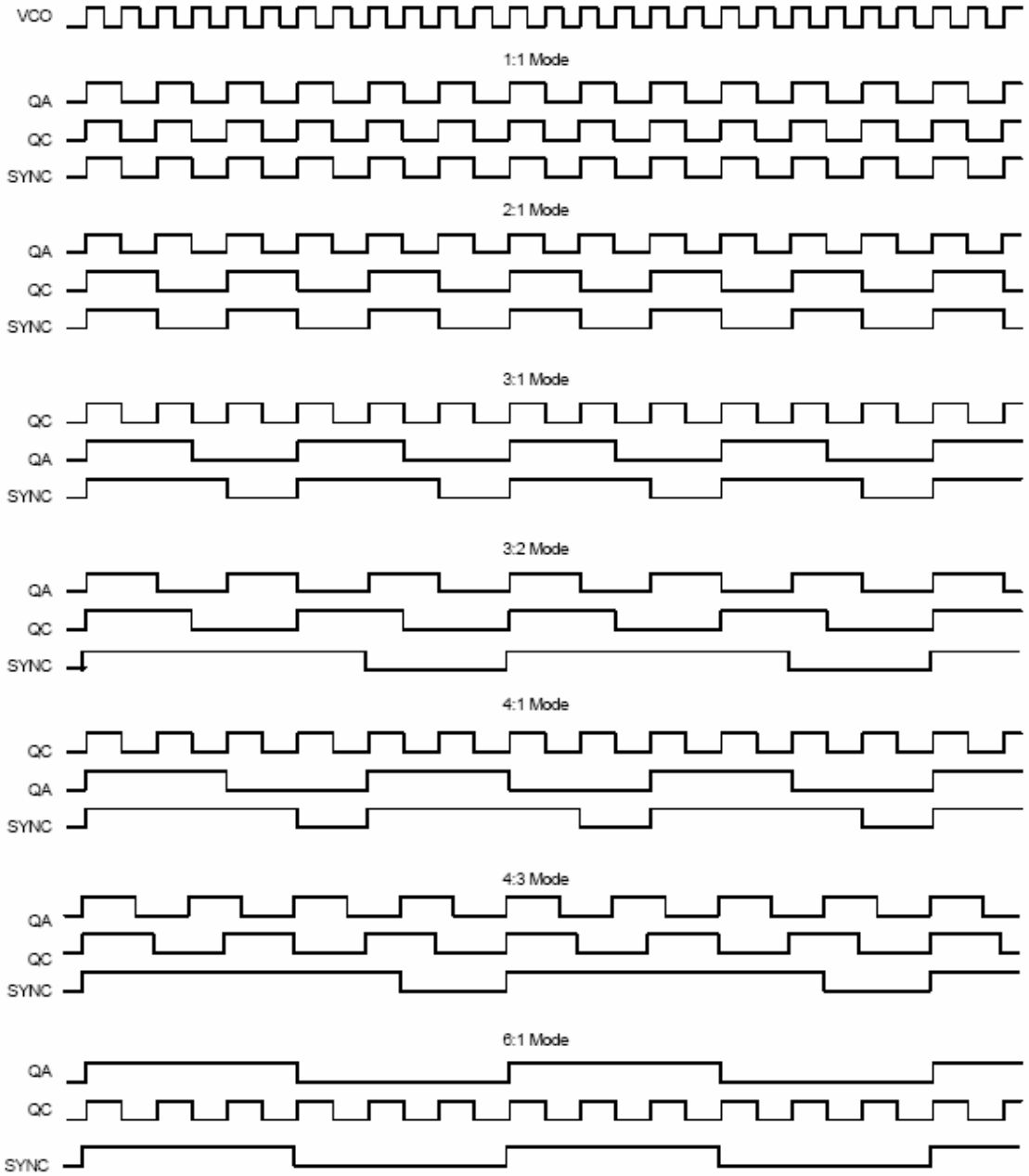

Figure 1.

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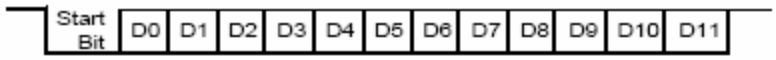
Power Management

The individual output enable/freeze control of the ASM5I9773A allows the user to implement unique power management schemes into the design. The outputs are stopped in the logic '0' state when the freeze control bits are activated. The serial input register contains one programmable freeze enable bit for 12 of the 14 output clocks. The QC0 and FB_OUT outputs can not be frozen with the serial port, this avoids any potential lock up situation, should an error occur in the loading of the serial data. An output is frozen when a logic '0' is programmed and enabled when a logic '1' is written. The enabling and freezing of individual outputs is done in such a manner as to eliminate the possibility of partial "runt" clocks. The serial input register is programmed through the SDATA input by writing a logic '0' start bit followed by 12 NRZ freeze enable bits. The period of each SDATA bit equals the period of the free running SCLK signal. The SDATA is sampled on the rising edge of SCLK.



D0-D3 are the control bits for QA0-QA3, respectively
D4-D7 are the control bits for QB0-QB3, respectively
D8-D10 are the control bits for QC1-QC3, respectively
D11 is the control bit for SYNC

Figure 2.

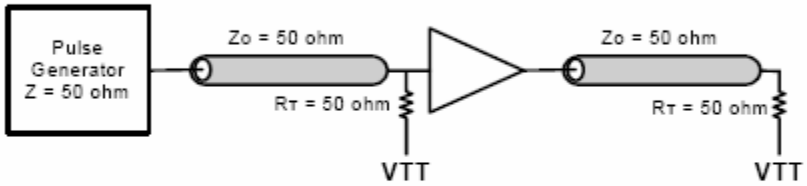


Figure 3. LVCMOS_CLK AC Test Reference for V_{DD} = 3.3V/2.5V

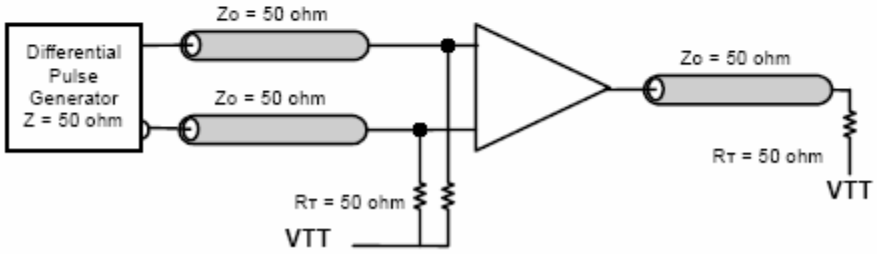


Figure 4. PECL_CLK AC Test Reference for V_{DD} = 3.3V/2.5V

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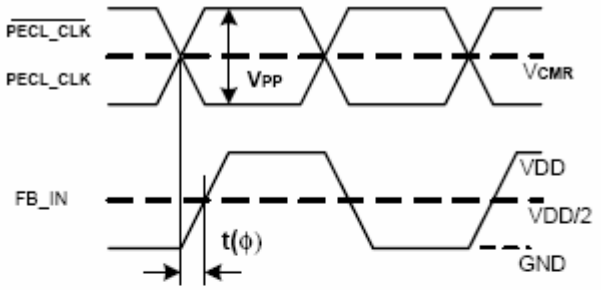


Figure 5. LVPECL Propagation Delay t(ϕ), Static Phase Offset

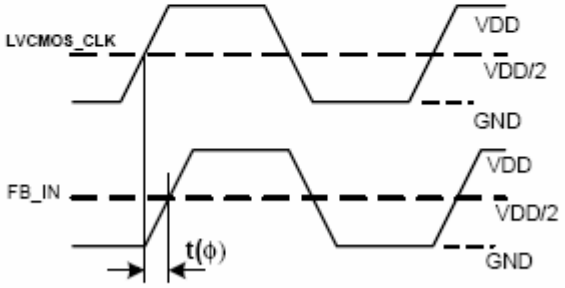
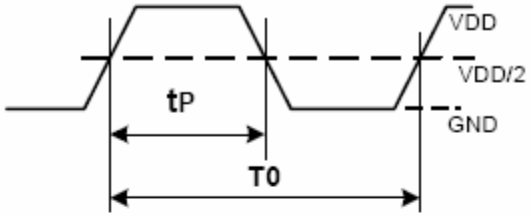


Figure 6. LVCMOS Propagation Delay t(ϕ), Static Phase Offset



DC = tP / T0 x 100%

Figure 7. Output Duty Cycle (DC)

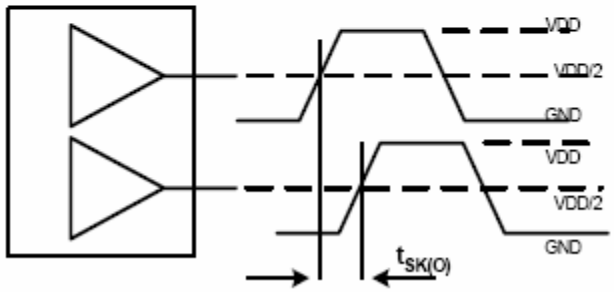


Figure 8. Output-to-Output Skew, $t_{sk(O)}$

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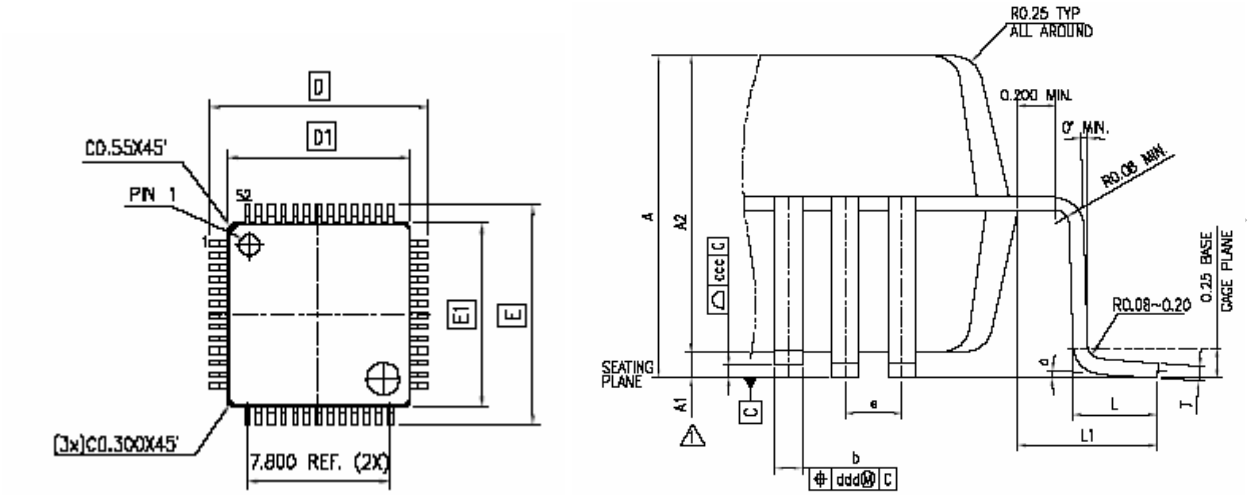
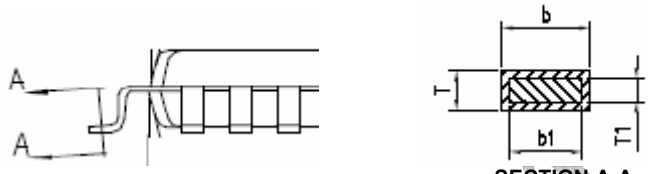
Package Information

52-lead TQFP Package





SECTION A-A

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	…	0.0472	…	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.4646	0.4803	11.8	12.2
D1	0.3898	0.3976	9.9	10.1
E	0.4646	0.4803	11.8	12.2
E1	0.3898	0.3976	9.9	10.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0102	0.0150	0.26	0.38
b1	0.0106	0.0130	0.27	0.33
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.0256 BASE		0.65 BASE	

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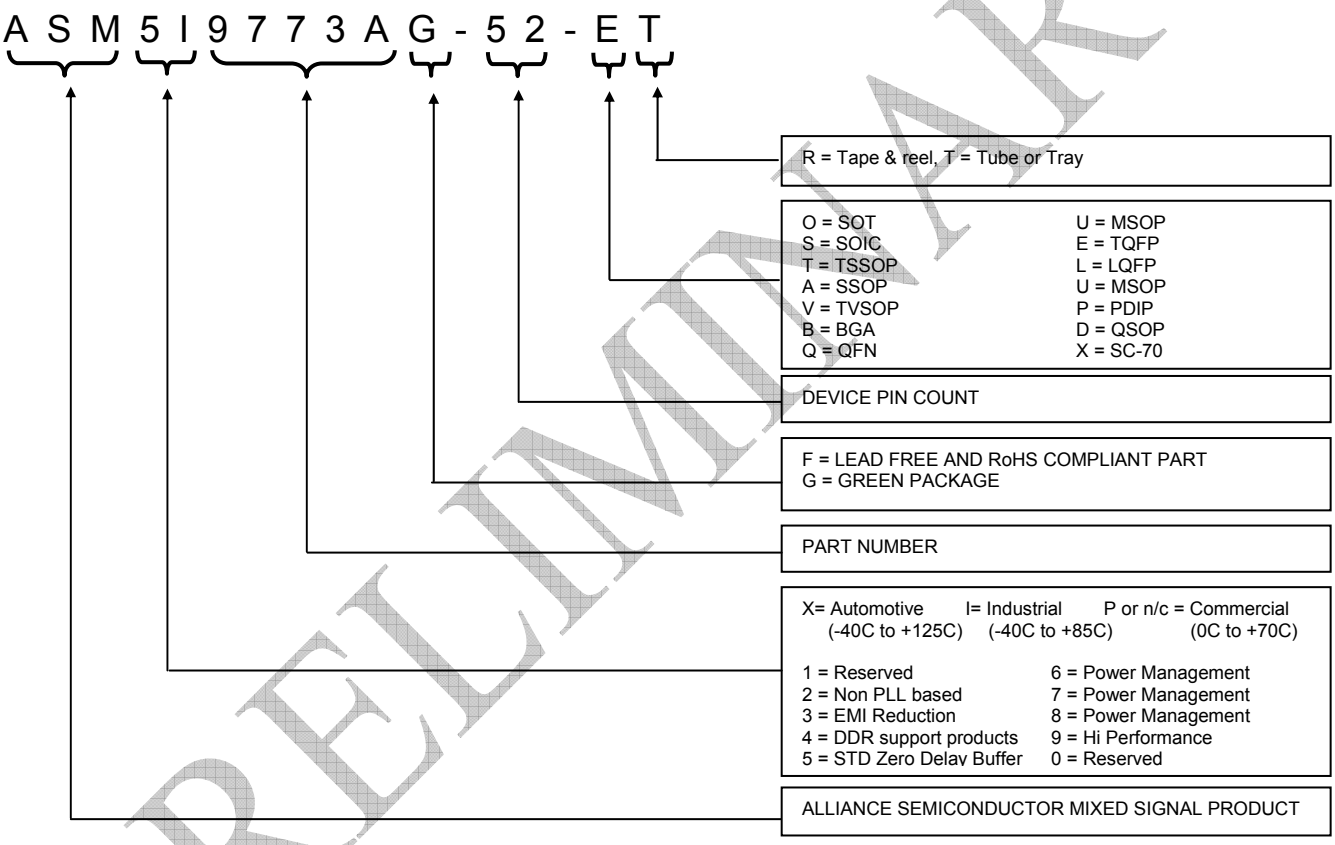
Ordering Information

Part Number	Marking	Package Type	Operating Range
ASM5I9773A-52-ET	ASM5I9773A	52-pin TQFP, Tray	Industrial
ASM5I9773A-52-ER	ASM5I9773A	52-pin TQFP – Tape and Reel	Industrial
ASM5I9773AG-52-ET	ASM5I9773AG	52-pin TQFP, Tray, Green	Industrial
ASM5I9773AG-52-ER	ASM5I9773AG	52-pin TQFP – Tape and Reel, Green	Industrial

Device Ordering Information


A S M 5 I 9 7 7 3 A G - 5 2 - E T
R = Tape & reel, T = Tube or Tray
O = SOT
S = SOIC
T = TSSOP
A = SSOP
V = TVSOP
B = BGA
Q = QFN
U = MSOP
E = TQFP
L = LQFP
U = MSOP
P = PDIP
D = QSOP
X = SC-70
DEVICE PIN COUNT
F = LEAD FREE AND RoHS COMPLIANT PART
G = GREEN PACKAGE
PART NUMBER
X= Automotive (-40C to +125C)
I= Industrial (-40C to +85C)
P or n/c = Commercial (0C to +70C)
1 = Reserved
2 = Non PLL based
3 = EMI Reduction
4 = DDR support products
5 = STD Zero Delay Buffer
6 = Power Management
7 = Power Management
8 = Power Management
9 = Hi Performance
0 = Reserved
ALLIANCE SEMICONDUCTOR MIXED SIGNAL PRODUCT

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Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

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Document Version: 0.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003

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